

**UNITED STATES DEPARTMENT OF COMMERCE****Patent and Trademark Office**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/902,809	07/30/97	SCHUEGRAF	K 303.278US1

MM21/0508  
SCHWEGMAN LUNDBERG WOESSNER & KLUTH  
P O BOX 2938  
MINNEAPOLIS MN 55402

EXAMINER

NADAV, O

ART UNIT PAPER NUMBER

2811

DATE MAILED:05/08/00

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

# Advisory Action

Application No.  
08/902,809

Applicant(s)  
Schuegraf et al

Examiner  
ORI NADAV

Group Art Unit  
2811



THE PERIOD FOR RESPONSE: [check only a) or b)]

- a) ☒ expires 3 months from the mailing date of the final rejection.
- b) ☐ expires either three months from the mailing date of the final rejection, or on the mailing date of this Advisory Action, whichever is later. In no event, however, will the statutory period for the response expire later than six months from the date of the final rejection.

Any extension of time must be obtained by filing a petition under 37 CFR 1.136(a), the proposed response and the appropriate fee. The date on which the response, the petition, and the fee have been filed is the date of the response and also the date for the purposes of determining the period of extension and the corresponding amount of the fee. Any extension fee pursuant to 37 CFR 1.17 will be calculated from the date of the originally set shortened statutory period for response or as set forth in b) above.

- ☐ Appellant's Brief is due two months from the date of the Notice of Appeal filed on \_\_\_\_\_ (or within any period for response set forth above, whichever is later). See 37 CFR 1.191(d) and 37 CFR 1.192(a).

Applicant's response to the final rejection, filed on Feb 2, 2000 has been considered with the following effect, but is NOT deemed to place the application in condition for allowance:

- ☐ The proposed amendment(s):
- ☐ will be entered upon filing of a Notice of Appeal and an Appeal Brief.
  - ☐ will not be entered because:
    - ☐ they raise new issues that would require further consideration and/or search. (See note below).
    - ☐ they raise the issue of new matter. (See note below).
    - ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal.
    - ☐ they present additional claims without cancelling a corresponding number of finally rejected claims.

NOTE:

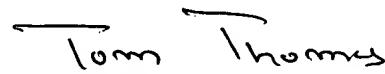
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

- ☐ Applicant's response has overcome the following rejection(s):

\_\_\_\_\_  
\_\_\_\_\_

- ☐ Newly proposed or amended claims \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment cancelling the non-allowable claims.
- ☒ The affidavit, exhibit or request for reconsideration has been considered but does NOT place the application in condition for allowance because:  
See attachment
- ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
- ☒ For purposes of Appeal, the status of the claims is as follows (see attached written explanation, if any):
- Claims allowed: None
- Claims objected to: None
- Claims rejected: 23-31 and 36-44

- ☐ The proposed drawing correction filed on \_\_\_\_\_ ☐ has ☐ has not been approved by the Examiner.
- ☐ Note the attached Information Disclosure Statement(s), PTO-1449, Paper No(s). \_\_\_\_\_
- ☐ Other

  
Tom Thomas  
Supervisory Patent Examiner  
Technology Center 2800

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## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant argues on pages 2-3 that Li teaches the term 'active area' as being anything in the semiconductor device that lies between areas of field oxides, including the gate oxide and features on the gate oxide. However, Li specifically teaches "active area of silicon", which means that an active area comprises silicon. Silicon, as well known in the art, can not be confused with gate oxide or a gate electrode. Therefore, Li does not support applicant's contention that the term 'active area' is being anything in the semiconductor device that lies between areas of field oxides, including the gate oxide and features on the gate oxide.
2. Applicant provide 5 separate arguments on page 4 that an artisan would come to the conclusion that active area 215 is an oxide area. However, these arguments were adequately addressed in previous office actions.
3. Applicant argues in reply to paragraph 12 that the examiner stated that applicant said that an active area mask comprises an active area and an insulating area. However, the examiner did not state that applicant said that an active area mask comprises an active area and an insulating area. The examiner stated that "applicant does not define layer 215 as an active area mask. Applicant defines layer 215 as an active area, whose meaning is well known in the art.

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Therefore, even if applicant's allegations regarding the definition of an 'active area mask' are correct, there is no support in the specification for an active area 215 being an oxide layer. In any event, the parameters of an active area mask should be described in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention".

4. Applicant argues in reply to paragraph 13 that the examiner stated that the invention is not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. However, the examiner never stated in paragraph 13 that the invention is not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention.

5. Applicant argues in reply to paragraph 17 that an artisan would recognize layer 215 as an oxide layer, because applicant demonstrated that an active area can be anything in the semiconductor device that lies between areas of field oxides, including the gate oxide and features on the gate oxide, and it is further consistent with CMOS structure. However, applicant did not demonstrate that an active area can be anything in the semiconductor device that lies between areas of field oxides, including the gate oxide and features on the gate oxide.

Furthermore, in addition to the response presented in previous office action, applicant did not categorize the claimed invention as a CMOS device. Applicant described the disadvantages of

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prior art CMOS devices, and one can not hypothesize that the invented structure comprises all the known elements of a CMOS device. In fact, the claimed invention does not incorporate all the conventional elements of a CMOS device, because it would incorporate the same disadvantages as the prior art CMOS devices.

6. The rest of applicant's arguments were adequately addressed in previous office action.

**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is (703) 308-8138. The

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Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time)  
Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to  
the **Technology Center Receptionists** whose telephone number is **308-0956**

Ori Nadav, Ph.D.

May 4, 2000

Tom Thomas

Tom Thomas  
Supervisory Patent Examiner  
Technology Center 2000